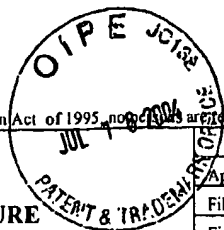


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				Filing Date	August 17, 2001
				First Named Inventor	Serge Lasserre
				Group Art Unit	2188
				Examiner Name	Reginald G. Bragdon
Sheet	1	of	1	Attorney Docket No.	TI-31354

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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	BA	EP	0 529 217 A	Motorola Inc.	3/3/93		
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RGB	CA	IBM Corp.; Use of Dirty, Buffered, and Invalidate Bits for Cache Operations, IBM Technical Disclosure Bulletin; New York, US, vol. 35, no. 1A, 1 June 1992, pg. 124.			
RGB	CB	IBM Corp.; Low End Parallel Bus Memory Refresh Activated Bus Timeout Control, IBM Technical Disclosure Bulletin; New York, US, vol. 31, no. 3, 1 August 1988, pgs. 90-92.			
	CC				
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Examiner Signature	Reginald G. Bragdon	Date Considered	10-5-2004
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